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Box PATENT APPLICATION

Sir:
Transmitted herewith for filing is the patent application of:

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For: **SEMICONDUCTOR ARRANGEMENT**

This application includes:

11 pages: specification and claims
11 sheets of drawings
___ photographs

Also enclosed is:
X Declaration and Power of Attorney
___ Information Disclosure Statement pursuant to 37 CFR 1.56.

The filing fee has been calculated as shown below:

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APPLICATION FOR LETTERS PATENT
OF THE UNITED STATES

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TITLE OF INVENTION: SEMICONDUCTOR ARRANGEMENT

TO WHOM IT MAY CONCERN, THE FOLLOWING IS
A SPECIFICATION OF THE AFORESAID INVENTION

SEMICONDUCTOR ARRANGEMENT

BACKGROUND OF THE INVENTION

This invention relates generally to semiconductor packages and to modules having such packages.

As is known in the art, semiconductor packing is typically performed by forming a plurality of identical integrated circuit chips on a semiconductor wafer. Also formed on the wafer during the fabrication of the chips is a plurality of scribe lines, or kerfs, which separate the chips. The integrated circuit chip definition is essentially complete at this wafer processing level. Some modification using electrical or laser fusing is possible such as spare, or redundant element replacement and circuit parameter (e.g., resistance) trimming, but this is limited to electrical elements with a single chip.

The wafer is then tested. The individual chips are then diced (i.e., separated) by scribing and breaking along the scribe lines. The now separated chips are individually packaged, re-tested, and sold as individual packaged chips. Typically, these individually packaged chips are mounted to a printed circuit board (PCB). For example, when the chips are Dynamic Random Access Memories (DRAMs), the individual packaged chips are mounted to a PCB to provide a memory module, such as a Single In-Line Memory Module (SIMM), Dual In-Line Memory Module (DIMM), or Rambus In-Line Memory Module (RIMM).

As is also known in the art, a DRAM chip typically includes two regions: memory array regions; and, non-memory array regions. These non-memory array regions are generally referred to as regions peripheral to the array regions or merely as peripheral regions. More particularly, referring to FIG. 1, a semiconductor wafer 10 is shown having a plurality of identical semiconductor chips 12. The fabricated chips 12 are then separated along the scribe lines 14. The borders of the scribe lines 14 shown more clearly in FIG. 2 and are designated as 14a, 14b, such FIG. 2 showing a portion of the wafer 10 shown in FIG. 1. Thus, an exemplary one of the chips 12 is shown in detail in FIG. 2 to include memory array regions, here four memory array regions 16 and peripheral regions 17. Each array region 16 includes the DRAM memory cells and associated row and column decoders, not shown. The peripheral regions 17 typically include decoders and sense amplifiers, not shown. Also included in the peripheral region 17 of each chip 12 is, in this example, a pair of voltage generators 20. Also

disposed in the peripheral regions 17 are power busses 22 which electrically interconnect the voltage generators 20 to the array regions 16. In a conventional DRAM semiconductor chips, the voltage generators 20 occupy up to several percent of the total chip 12.

SUMMARY OF THE INVENTION

In accordance with the present invention, a semiconductor package is provided. The package includes a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon. The chips have separating regions between them. The fractional portion of the wafer has a plurality of electrical contacts electrically connected to the chips. The package also includes an electrical conductor to electrically connect the plurality of electrical contacts electrically interconnecting such chips with portions of the electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer.

With such an arrangement, rather than have each individual chip in a separate package, the chips are designed for module granularity enabling the entire fractional portion of the wafer (i.e., portions thereof which are not used in the circuitry of the individual chips) to be utilized in an optimum manner.

In accordance with one embodiment, a semiconductor package is provided. The package includes a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon. The chips have separating regions between them. The fractional portion of the wafer has a plurality of electrical contacts electrically connected to the chips. The package also includes a dielectric having an electrical conductor thereon. The electrical conductor electrically connects the plurality of electrical contacts to electrically interconnect such chips with portions of the electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer.

In accordance with the present invention, a semiconductor package is provided. The package includes a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon. The chips have separating regions between them. Peripheral electrical components are disposed in the separating regions. The package also includes an electrical conductor to electrically connect the plurality of electrical contacts to electrically interconnect such chips with peripheral electrical components

In accordance with one embodiment of the invention, a semiconductor memory is provided. The memory includes a fractional portion of a semiconductor wafer. The

fractional portion of the wafer has a plurality of integrated circuit chips. Each one of such chips has a memory array region. The chips have separating regions between them. A periphery electrical component is disposed on the fractional portion of the wafer in one of the separating regions An electrical interconnect is provided for electrically connecting the chip to the periphery electrical component.

With such an arrangement, the periphery components are added to the memory in a more efficient manner as compared to a module having only a single integrated circuit memory chip. Several benefits of this efficiency are: an averaging of elements to reduce variations; sharing of chip elements to increase the number of chips per wafer; selecting circuit options; and, wiring across the chips within the module.

In accordance with another embodiment of the invention, a semiconductor memory package is provided having a fractional portion of a semiconductor wafer. The fractional portion of the wafer has a plurality of integrated circuit chips. Each one of such chips has a memory array region. The chips have separating regions therebetween. A periphery electrical component is disposed in one of the separating regions. An electrical interconnect is provided for electrically connecting the chip to the peripheral electrical component.

In accordance with another embodiment of the invention, a semiconductor packaging arrangement, or module, is provided. The module includes a printed circuit board having an electrical interconnect thereon and a semiconductor package mounted to the printed circuit board. The semiconductor package includes a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer. The fractional portion of the wafer has a plurality of electrical contacts electrically connected to the chips. The package also includes a dielectric having an electrical conductor thereon. The electrical conductor are electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips with portions of the electrical conductor spanning the regions in the fractional portion of the wafer. A connector is provided for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board. In accordance with another embodiment of the invention, a semiconductor memory is provided having a fractional portion of a semiconductor wafer. The fractional portion has a plurality of integrated circuit chips. Each one of such chips has a memory array region. The chips have separating regions therebetween. A periphery electrical component is disposed in one

of the separating regions. An electrical interconnect electrically connects the chips to the periphery electrical component.

With such an arrangement, the same periphery electrical component is shared by the chips.

In accordance with still another embodiment of the invention, a method is provided for providing a packaging arrangement. The method includes providing a semiconductor wafer having formed thereon a plurality of semiconductor chips, such chips being separated by regions in the wafer, such wafer having a plurality of electrical contacts electrically connected to the chips. A dielectric member is provided having thereon an electrical conductor. The dielectric member is positioned over the wafer with the electrical conductor being disposed on the plurality of electrical contacts and with such electrical conductor spanning the regions. The positioned dielectric member is connected to the semiconductor wafer to provide a unitary structure. The unitary structure is separated into a plurality of packages, each one of the packages having a plurality of the chips with the electrical contacts of the plurality of the chips in such package being electrically connected to a corresponding portion of the spanning electrical conductor in such package.

In one embodiment, a printed circuit board is provided having an electrical interconnect thereon; and, electrically interconnecting the electrical conductor of the package to the electrical interconnect.

The details of one or more embodiments of the invention are set forth in the accompanying drawings and the description below. Other features, objects, and advantages of the invention will be apparent from the description and drawings, and from the claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is a plan view, simplified sketch of a semiconductor wafer having a plurality of integrated circuit chips according to the PRIOR ART;

FIG. 2 is an exploded view of a portion of the wafer of FIG. 1;

FIG. 3 is a plan view, simplified sketch of a semiconductor wafer having a plurality of integrated circuit chips according to the invention;

FIG. 4 is an exploded view of a portion of the wafer of FIG. 3 having a plurality of the integrated circuit chips therein, such portion being enclosed in the arrow labeled 4-4 in FIG. 3;

FIG. 5 is a diagrammatical plan view of the portion of the wafer shown in FIG. 4 with a dielectric member disposed over such portion of the wafer and with such dielectric member having electrical conductors thereon in contact with electrical contacts on the chips in such portion of the wafer, such electrical conductors being shown using cross-hatching in FIG. 5;

FIG. 6 is an exploded, cross sectional view of the package of FIG. 5 such cross section being taken along line 6-6 in FIG. 5;

FIG. 7 is a cross sectional view of a semiconductor package according to the invention, such package having a separated, fractional portion of the wafer of FIGS. 5 and 6, and overlying fractional portion of the dielectric member of FIGS. 5 and 6;

FIG. 8 is a packaging assembly having the package of FIG. 7 connected to a portion of a printed circuit board according to the invention;

FIGS. 9A through 9D are plan views of a portion of a wafer with a dielectric member disposed over such portion of the wafer and with such dielectric member having electrical conductors thereon in contact with electrical contacts electrically connected to chips in such portion of the wafer, such electrical conductors being shown using cross-hatching, such FIGS. 9A through 9D showing such structure at various stages in the fabrication thereof to provide an interconnection of voltage generators formed thereon in accordance with the invention;

FIG. 9B' is an enlarged view of a portion of the wafer shown in FIG. 9B, such portion being enclosed by an arrow designated 9B'-9B' is FIG. 9B;

FIG. 9C' is an enlarged view of a portion of the wafer shown in FIG. 9B, such portion being enclosed by an arrow designated 9C'-9C' is FIG. 9B;

FIG. 10 is a schematic diagram of the structure shown in FIGS. 5, 6 and 7 according to the invention;

FIG. 11 is a schematic diagram of a structure according to an alternative embodiment of the invention;

FIG. 12 is a schematic diagram of the structure shown in FIG. 9D;

FIG. 13 is a schematic diagram of a structure according to an alternative embodiment of the invention; and

FIG. 14 is a schematic diagram of a structure according to an alternative embodiment of the invention.

Like reference symbols in the various drawings indicate like elements.

DETAILED DESCRIPTION

Referring now to FIG. 3, a semiconductor wafer 30 is shown having a plurality of identical integrated circuit chips, here DRAM chips 32 therein, is shown. The individual chips 32 are separated by separating regions, here scribe lines, or kerfs, 33. The borders of the scribe lines 33 are provided by crack-stop lines labeled 33a, 33b in an enlarged view of a portion of the wafer 30 shown in FIG. 4. Here, each one of the chips 32 includes, as with the chips 12 in FIG. 1, memory array regions 16, here four memory array regions 16 and non-array, or peripheral regions 17'. Here, in this example, each one of the chips 32 is identical in construction. Each array region 16 includes the DRAM memory cells and associated row and column decoders, not shown. It should be noted that periphery electrical components, here for example, voltage generators 48, are provided in the separating regions 33. More particularly, here a pair of the voltage generators 48 is disposed in a portion of the scribe line 33 adjacent to a corresponding one of the chips 32. Each pair of generators 48 is electrically connected to the adjacent, corresponding one of the chips 32, here for example to the array regions 40 of such chip 32, through power busses 50 formed on the chip 32, as indicated. It is noted that the generators 48 have electrical contacts 53, as shown more clearly in FIG. 4 and such electrical contacts are connected to the power busses 50.

Thus, a semiconductor wafer 30 is provided having formed thereon a plurality of semiconductor chips 32, such chips 32 being separated by separating regions 33 in the wafer 30, such wafer 30 having a plurality of electrical contacts 53.

Having fabricated the semiconductor wafer 30 as shown in FIGS. 3 and 4, a dielectric member 49, such as a thin printed circuit board, shown more clearly in FIG. 6 is provided with patterned electrical isolated electrical conductors 52 on one surface, here the inner surface of the dielectric member 49. The dielectric member 49 has an electrical contact 55 on the opposite, here outer surface thereof as indicated. The contact 55 is electrically connected to the electrical conductor 52 through via conductor 57. The dielectric member 49 may be a single member having the conductors formed on one surface of such member 50, as shown in FIGS. 5 and 6. The dielectric member 49 may be a multi-level, e.g., laminated member, having electrical conductors 52 in various dielectric layers thereof. In either case, one inner surface of the dielectric member 49 has at least one electrical conductor 52 which is electrically connected to the electrical contact 55 using a conductive via 57. The dielectric member 49, here having a diameter the same, or larger than the diameter of wafer 30, is placed over the surface of

the wafer 30 as indicated in FIG. 6, here the electrical conductors 52 are indicated by hatched lines for convenience.

Thus, a dielectric member 49 is provided having electrical conductors 52. The dielectric member 49 is positioned over the wafer 30 with the electrical conductors 52 being disposed on the plurality of electrical contacts 53 and with such electrical conductors 52 spanning the separating regions 33, as indicated in FIGS. 5 and 6. It is noted then that the electrical conductor 52 is thus electrically connected to the buss 50 through the contacts 53, as noted above.

Next, the positioned dielectric member 49 is connected to the semiconductor wafer 30 to provide a unitary structure 51 as indicated in FIG. 6. The unitary structure 51 is separated along the scribe lines 32 into a plurality of packages 60, and exemplary one of such packages 60 being shown in FIG. 7. Thus, in this example, each package 60 has a plurality, here four, of the chips 32 with the electrical contacts 53 of the four chips 32 in such package 60 being electrically connected the spanning electrical conductor 52. A schematic diagram of the package is shown in FIG. 10.

Next, a plurality of the packages 60 are arranged in a memory module 62 as indicated in FIG. 8. More particularly, here each memory module 62 includes a plurality of, here three, of the packages 60 shown in FIG. 7 and a printed circuit board 66 an electrical interconnects 68 thereon. The memory module 62 is fabricated by mechanically and electrically connecting the four packages 60 to the printed circuit board 66. More particularly, the electrical contacts 55 are disposed on and electrically connected to the electrical interconnects 68.

It is noted that with the packages 60 arranged as described in FIG. 7, each one of the voltage generators 48 is no longer assigned (i.e., electrically connected to) a single integrated circuit chip 32. Thus, while in the prior art each chip has its own generator, such generator must be calibrated individually to the particular chip. Here, however, by combining (i.e., electrically interconnecting) the generators 48 and then connecting them to all chips 32 in the package 60, the generator 48 produced voltages are the same for all chips 32 in the package 60. This results in less on-chip voltage variation and more constant timings during operation of the chips 32.A schematic diagram of package 60 is shown in FIGS. 5, 6 and 7 is shown in FIG. 10. Thus, it is noted that here each chip 32 has a pair of here identical voltage generators 48 formed in the separating regions 33, as described above in connection with FIGS. 4-8. As described above in connection with FIGS. 5 and 6, the voltage generators 48 have electrical contacts 53 which are

connected through the electrical conductor 52. Further, as noted above in connection with FIGS. 4-8 these electrical contacts are connected to the busses 50, as indicated schematically in FIG 10. Thus, with this average voltage provided by all of the here eight voltage generators is supplied to here all four chip 32.

Referring to FIG. 11, an alternative arrangement is shown where additional electrical conductors 52a, 52b and 52c are formed on the dielectric member 59 (FIG. 7) along with electrical conductor 52. Such an arrangement of the electrical conductors 52, 52a, 52b and 52c provides a more effective distribution of the voltages provided by the here eight voltage generators 48.

Referring now to FIGS. 9A-9D another embodiment of the invention is shown. Referring first to FIG. 9A, each one of the chips 32 has initially connected to it via bus 50 a pair of voltage generators 48a, 48b. Here, each one of the pair of generators 48a, 48b produces a different voltage. It is noted that here the dielectric 49 (described above in connection with FIGS, 5 and 6) is disposed on, and connected to, the wafer 30 as described above in connection with FIGS. 5 and 6. Here, however, the dielectric 49 has, in addition to electrical conductor 52, electrical conductors 52'a and 52'c arranged as shown. It is noted that electrical conductor 52 is in contact with electrical contacts 53 as described above in connection with FIGS. 5 and 6. Electrically connected to such conductor 52 are the conductors 52'a and 52'c. Thus, at this stage in the fabrication, electrical conductors 52'a and 52'c are electrically connected to contacts 53 and hence are electrically connected to bus 50 of each of the chips 32.

Next, and referring to FIG. 9B, the one of the pair of electrical contacts 53 in contact with voltage generator 48a is electrically disconnected from the bus 50, here by open-circuiting a laser fusible link to thereby produce gaps 50' as indicated more clearly in FIG. 9B'. Thus, the voltage generators 48a are electrically disconnected from the buses 50 while the voltage generators 48b remain electrically connected to such buses 50, as indicated.

Next, and referring to FIG. 9C, a laser is used to form open circuits 52' in the conductor 52, as indicated more clearly in FIG. 9C'. It is noted that there are a pair of gaps 52' to the right and to the left of each voltage generator 48a. Thus each voltage generator 48a is electrically disconnected from electrical contact 55. To put it another way, it should be noted that because of gaps 52', only the voltage generators 48b are electrically connected 53 together and such voltage generators 48a are electrically isolated from voltage generators 48b. Further, because of the gaps 50' described above

in connection with FIGS. 9B and 9B', the electrical conductor 52 with the gaps 52' is electrically connected to the electrical contact 55 and is electrically connected to only generator 48b.

Referring now to FIG. 9D, the structure shown in FIG. 9D is sawed along lines 33' and thereby separated into package of four electrically interconnected chips to form a plurality of packages 60'. The schematic diagram of one of the packages 60' is shown in FIG. 12.

It is noted that a similar procedure may be used where generator 48a is to be electrically connected to bus 50 and where generator 48b is to be electrically isolated from bus 50. The schematic diagram for such an arrangement is shown in FIG. 13.

From the above, it follows that other package arrangements may be provided. For example, referring to FIG. 14 package 60" has four similar voltage generators 48', one adjacent to a corresponding one of the four chips 32, are interconnected via conductor 52 to provide an average voltage to the chips 32 via busses 50. Thus, from the above it should be noted that because some memory packages 60, 60', 60" have configurations in which not all of the individual chips 32 are active at one time, with the arrangement according to the invention described above, the generators 48 in the package 60 may be shared between chips 32 in the package 60 thus improving the chip-count per wafer since the generator size may be reduced. Still further, because the generators 48, 48a, 48b need not be placed in the chip 32 but rather in the separating regions 33 between the chips 32, the number of chips 32 per wafer 30 (FIG. 3) may be increased. This arrangement also allows the capacitance of other chips within the package to stabilize the generated voltages with the memory package. Further, with this arrangement, the bus width on the chip may be reduced to thereby reduce chip area.

A number of embodiments of the invention have been described. Nevertheless, it will be understood that various modifications may be made without departing from the spirit and scope of the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of electrical components, each one being associated with, and adjacent to, a corresponding one of the chips.

2. The semiconductor recited in claim 1 wherein the electrical components are voltage generators.

3. The semiconductor recited in claim 2 wherein each one of the components is disposed in the separating region,

4. The semiconductor recited in claim 3 wherein the electrical components are voltage generators

5. The semiconductor recited in claim 1 wherein each one of the voltage generators has an electrical contact and wherein such package includes:

a dielectric member having an electrical conductor thereon, such electrical conductor being electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer.

6. A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

an electrical conductor electrically connecting the plurality of electrical selected one or ones of the electrical components to the chips with portions of the

electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer.

7. The semiconductor recited in claim 6 wherein each set having a plurality of different electrical components.

8. A method for forming a semiconductor, comprising:

providing a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

providing a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

providing an electrical conductor to electrically connect a selected one or ones of the electrical components to the chips with portions of the electrical conductor spanning the separating regions between the chips in the fractional portion of the wafer.

9. The method recited in claim 8 wherein each set is provided with a plurality of different electrical components.

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SEMICONDUCTOR ARRANGEMENT

ABSTRACT OF THE DISCLOSURE

A semiconductor packaging arrangement, or module, includes a printed circuit board having an electrical interconnect thereon and a semiconductor package mounted to the printed circuit board. The semiconductor package includes a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer. The fractional portion of the wafer has a plurality of electrical contacts electrically connected to the chips. The package also includes a dielectric member having an electrical conductor thereon. The electrical conductor are electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips with portions of the electrical conductor spanning the regions in the fractional portion of the wafer. A connector is provided for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board.

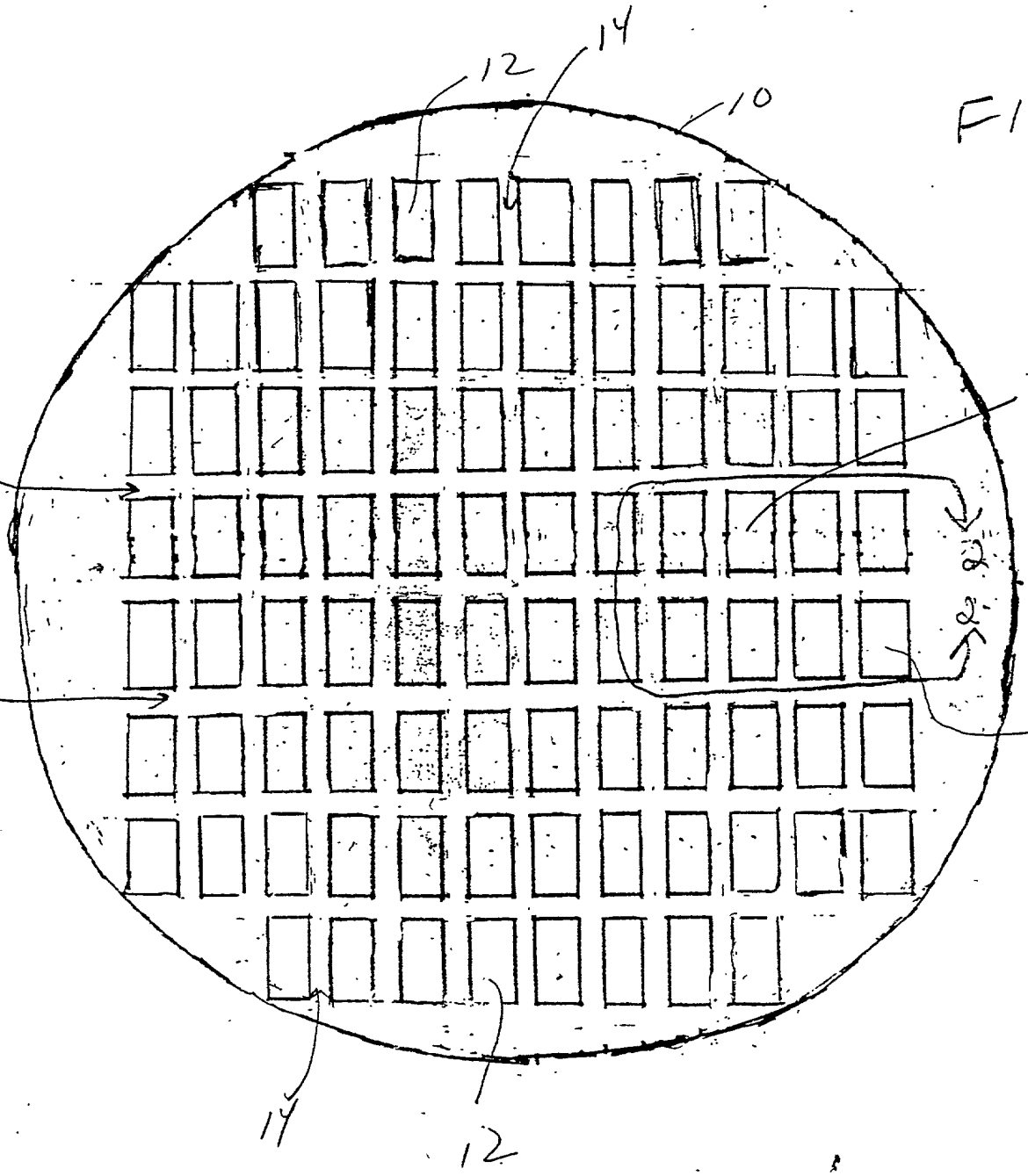
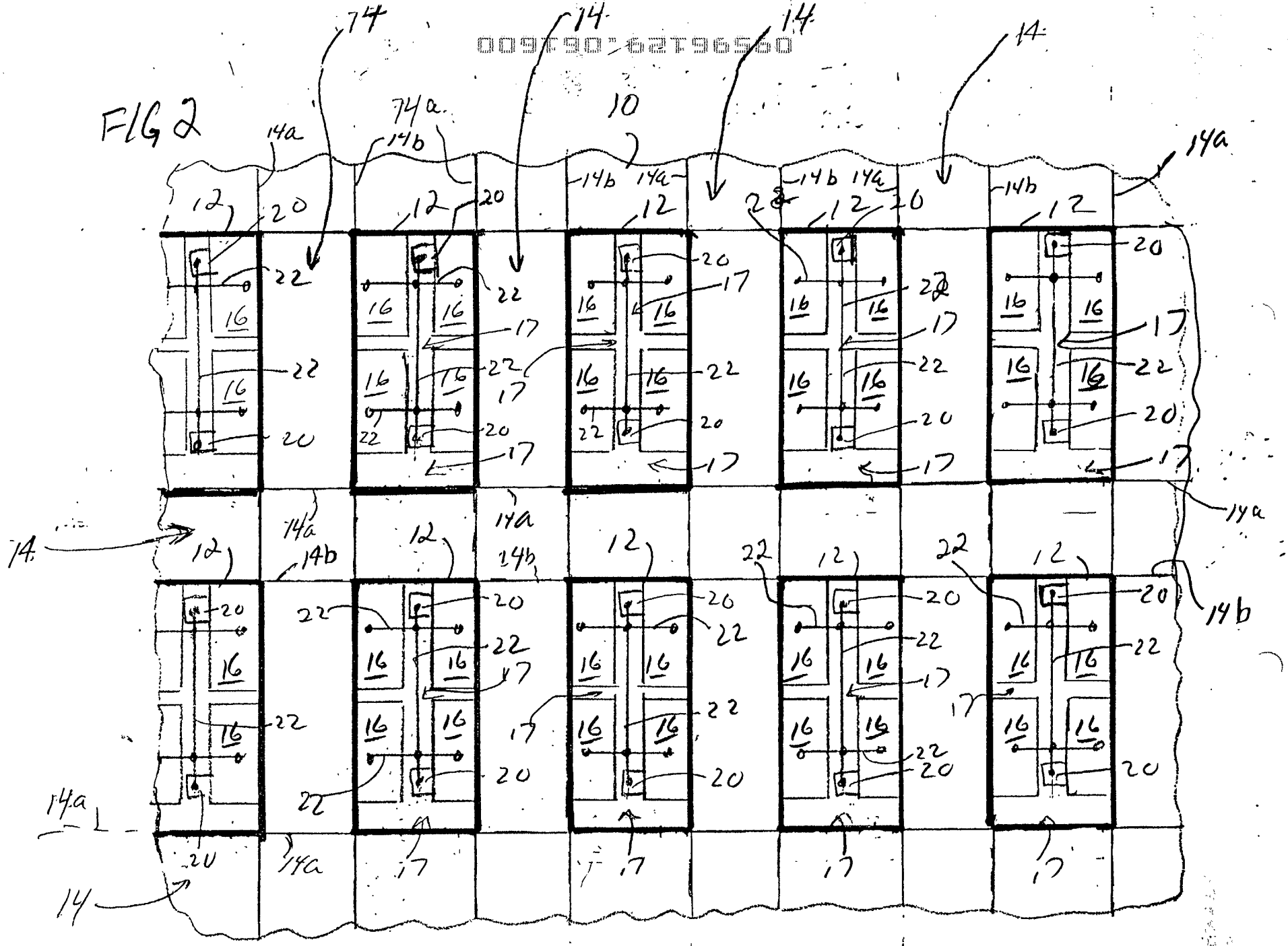


FIG. 1

FIG 2



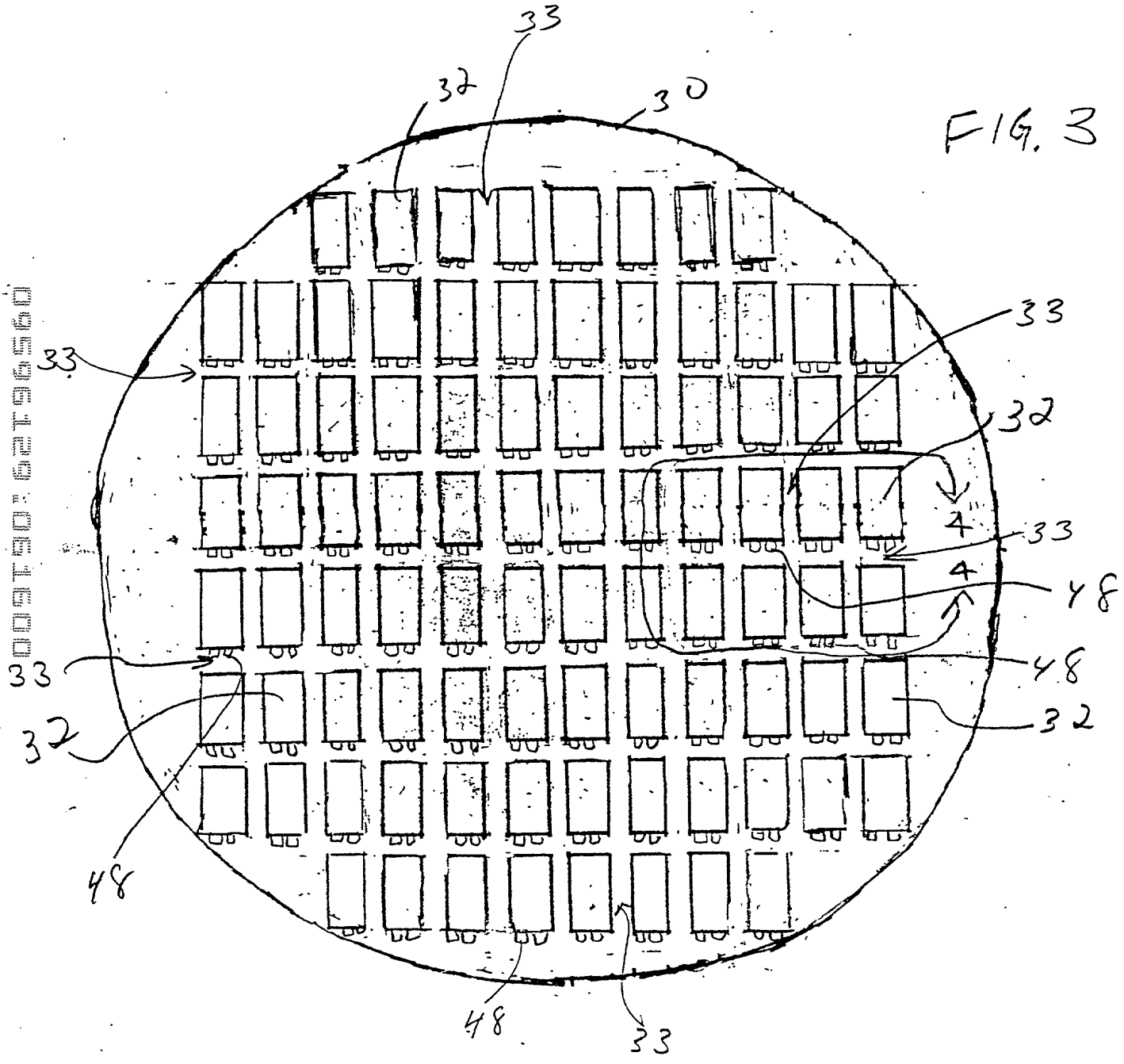


FIG. 3

FIG 4

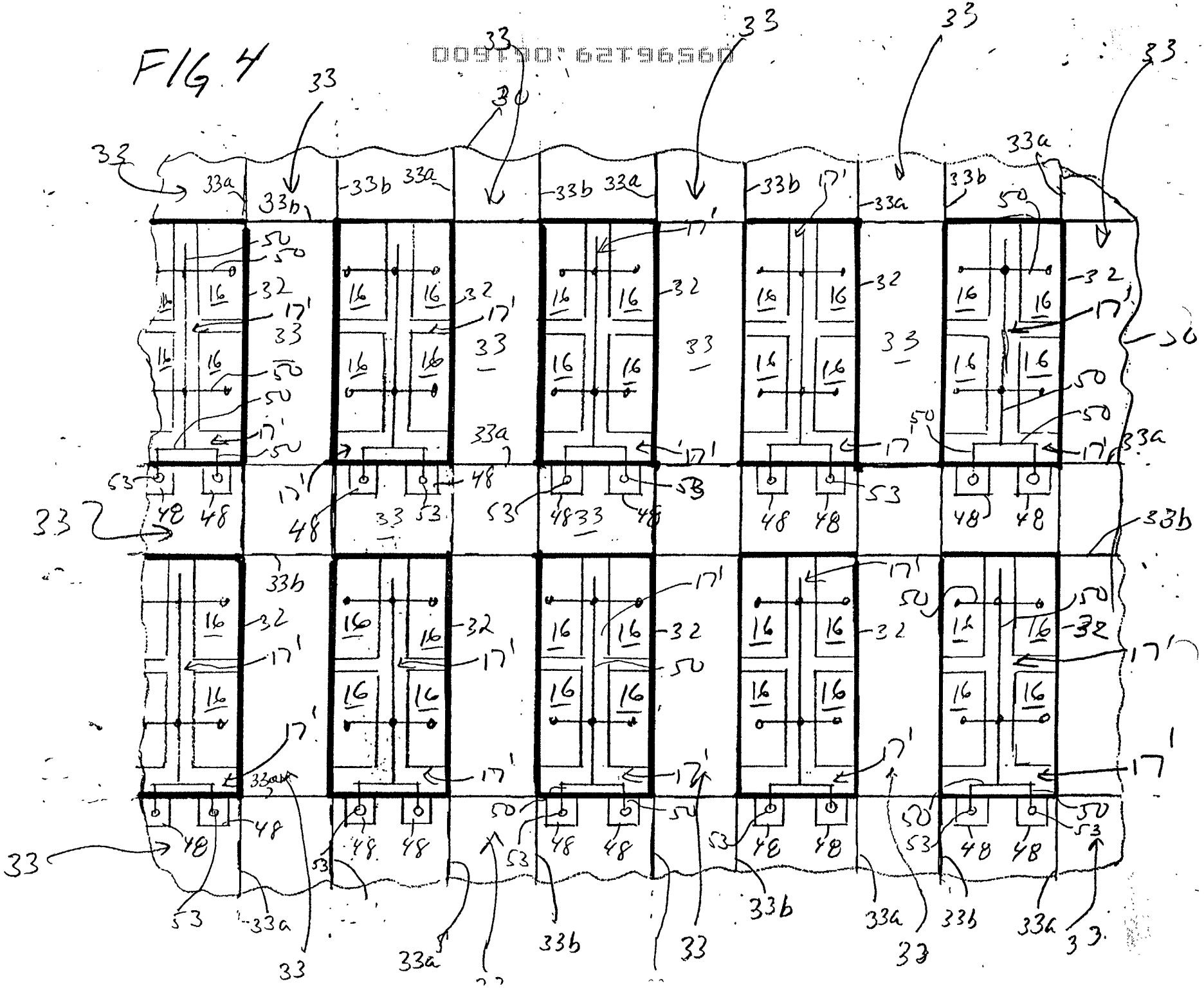
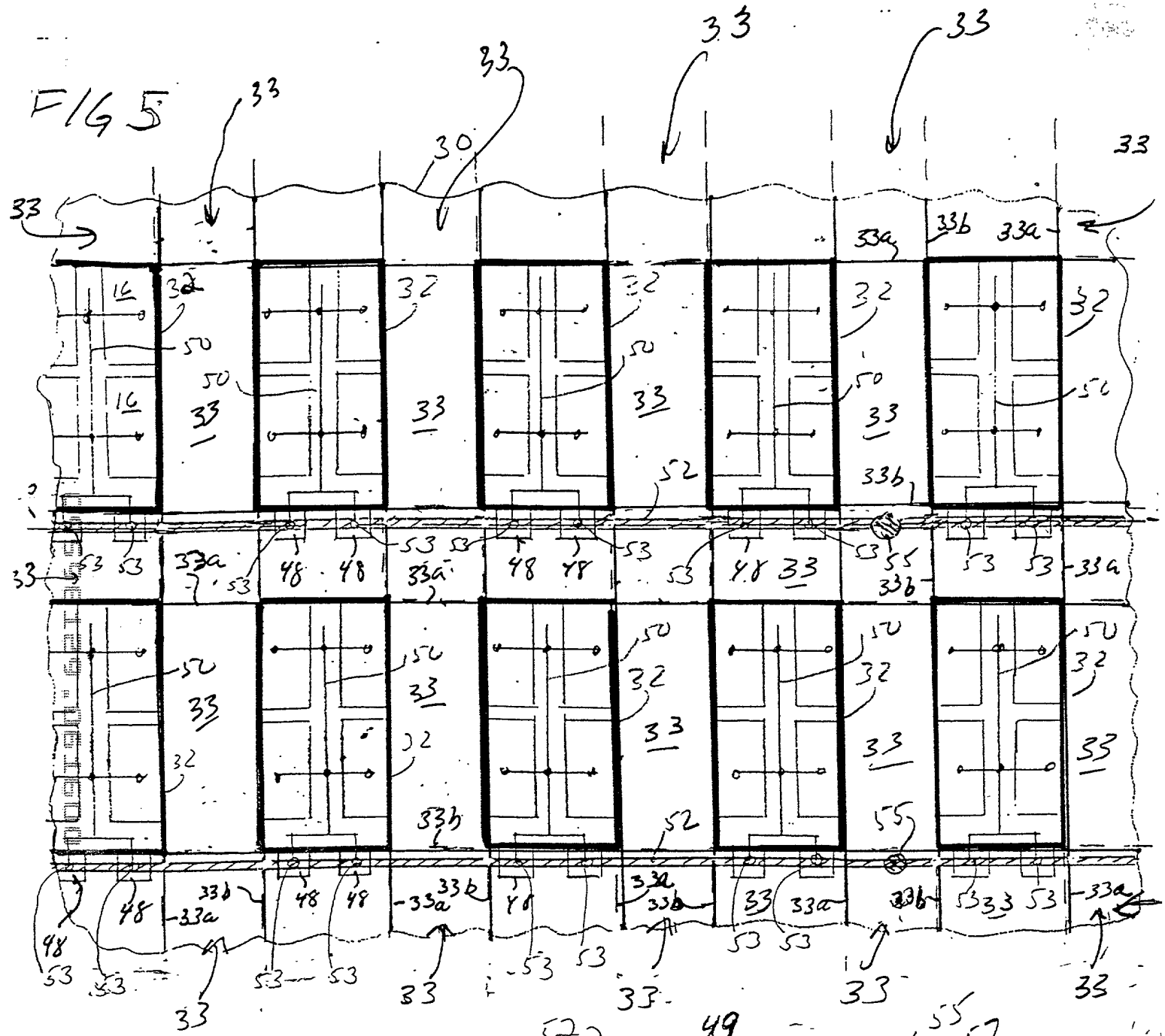


FIG 5



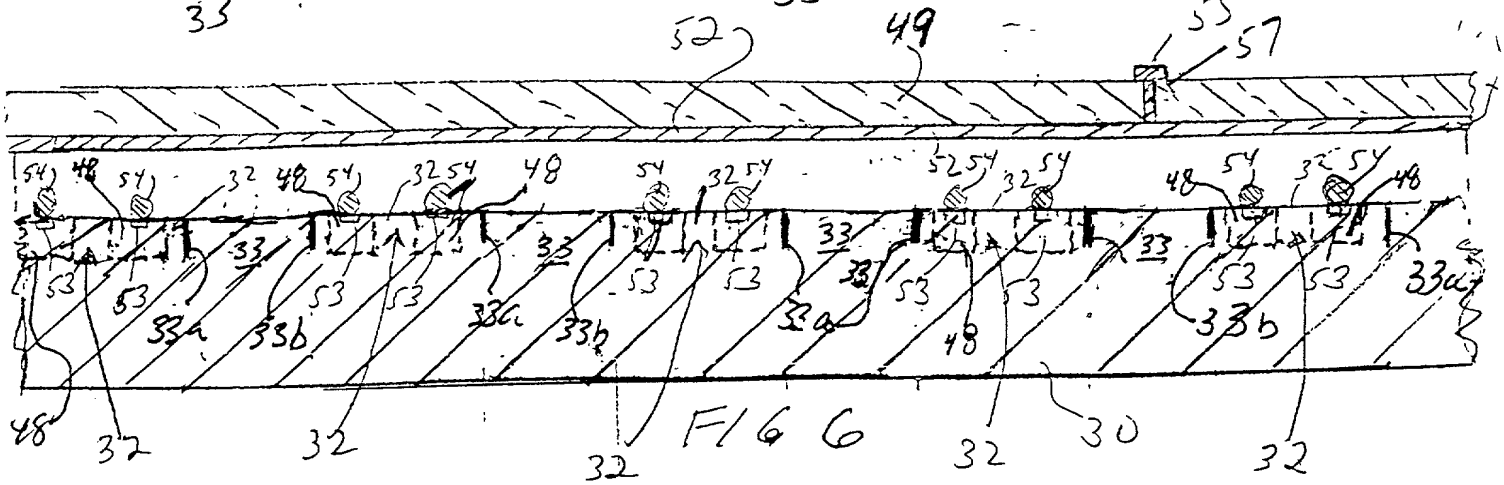


FIG 6

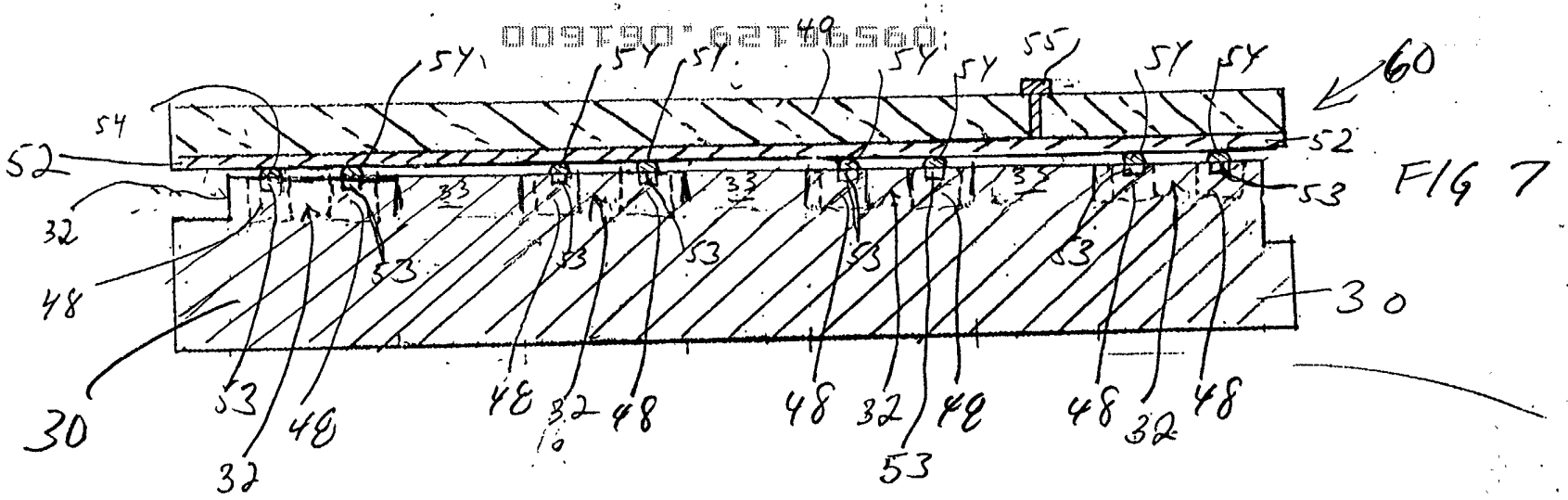


FIG 7

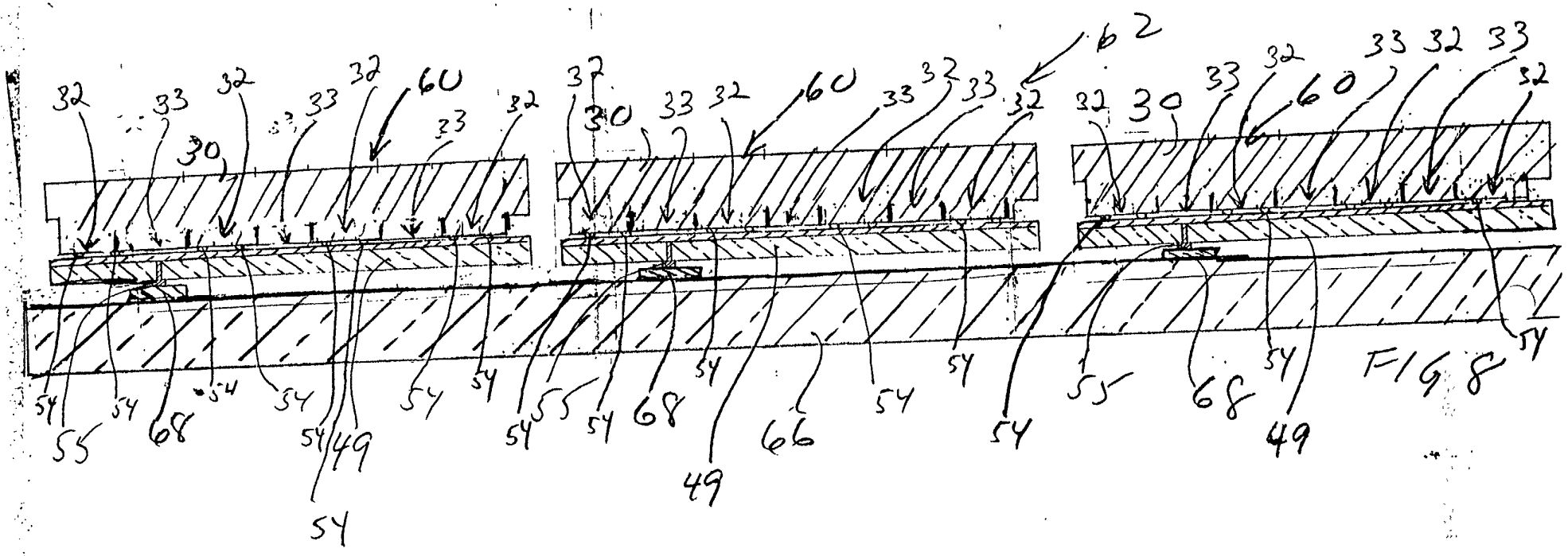


FIG 8

~~FIG 9~~

FIG 9A

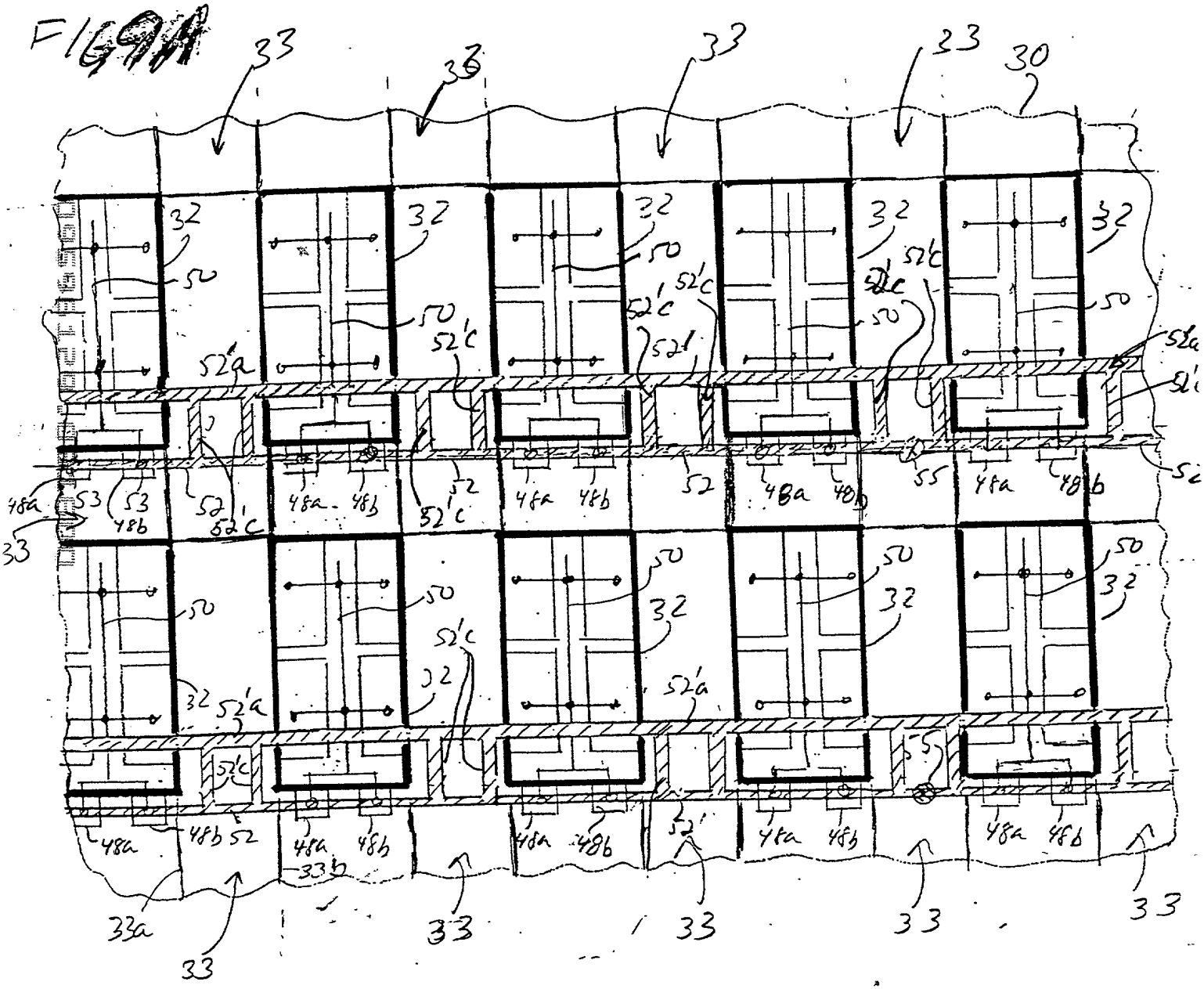


FIG 9B'

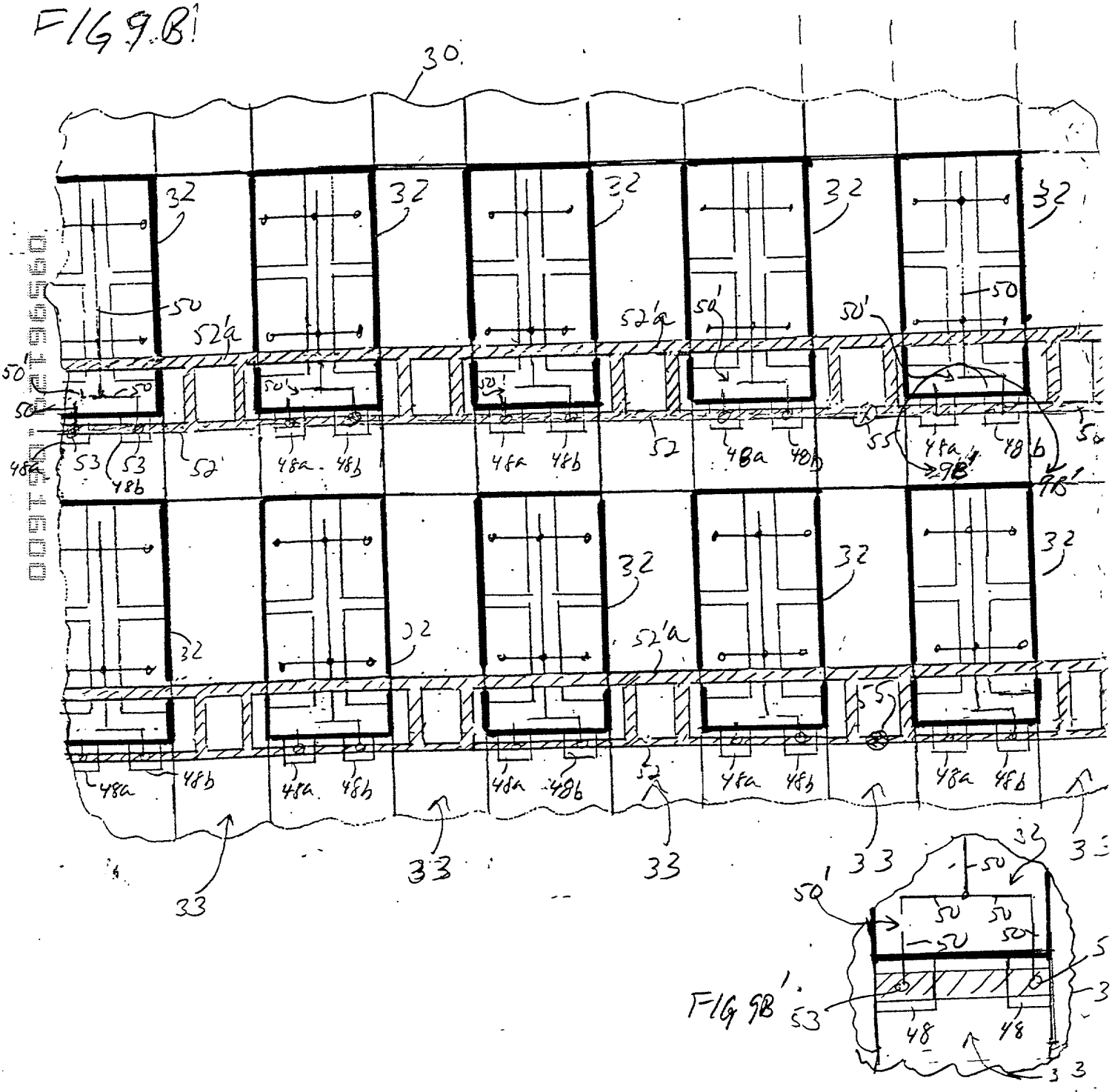


FIG 9B'

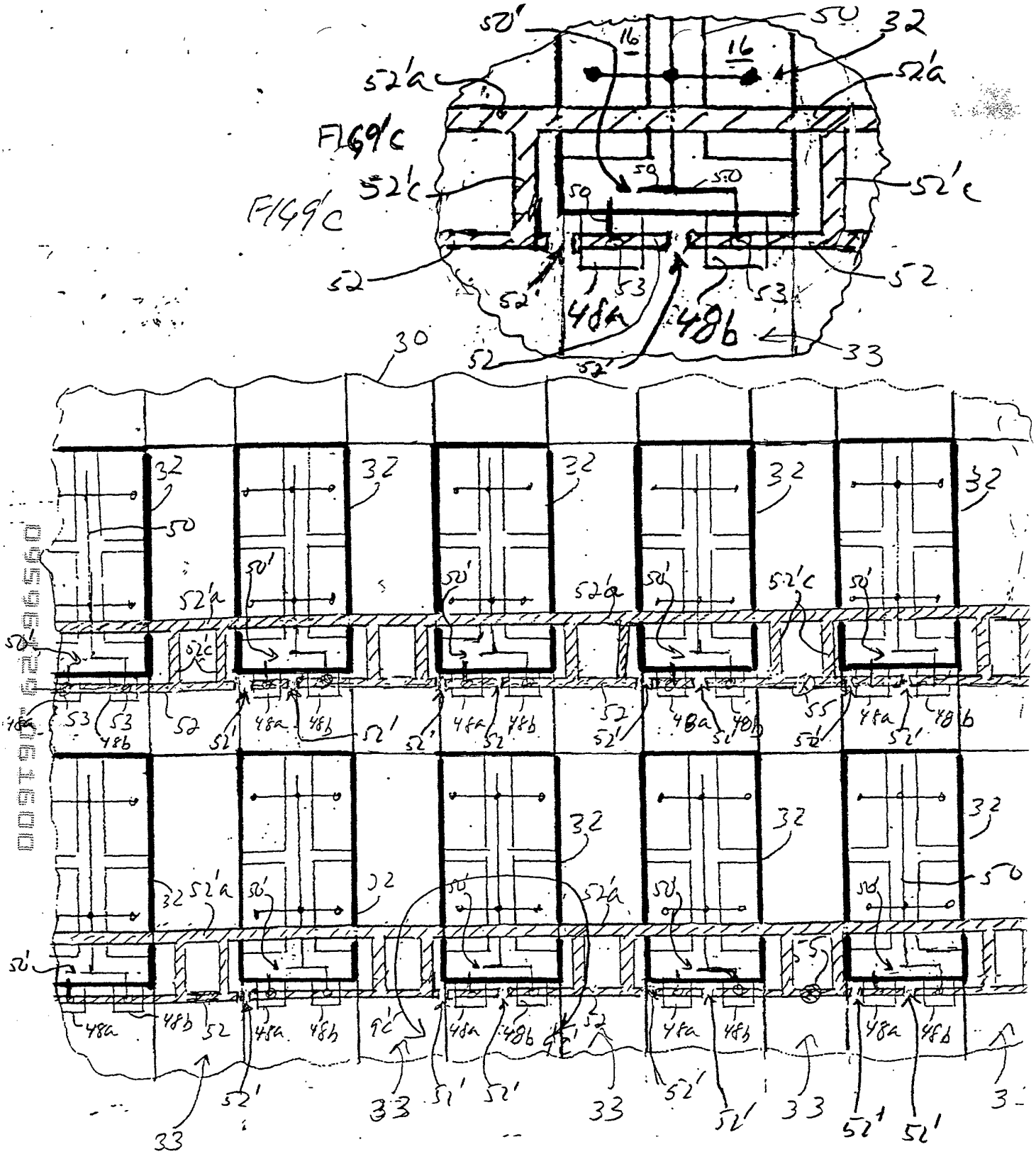
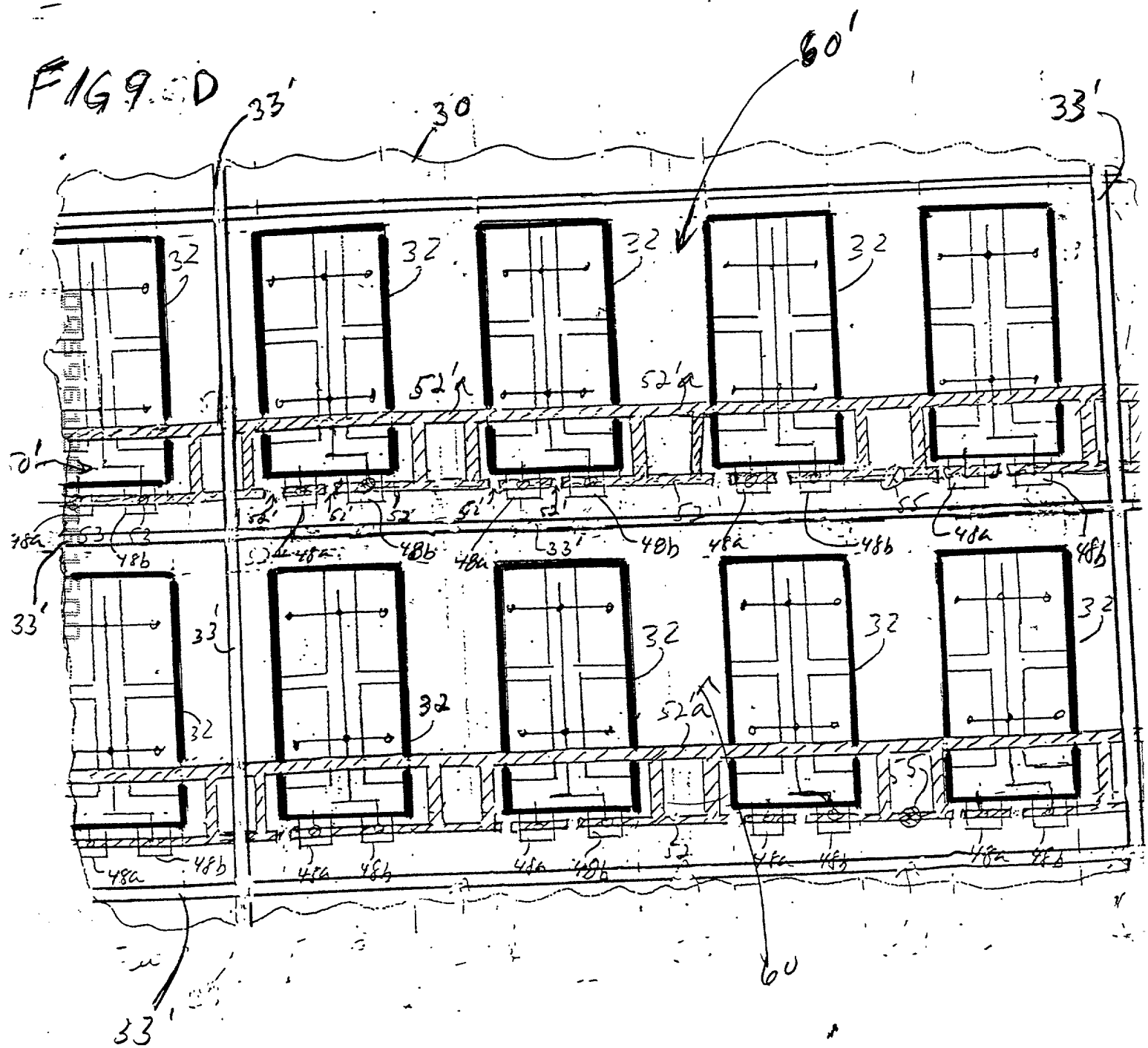


FIG 9C

FIG 9D



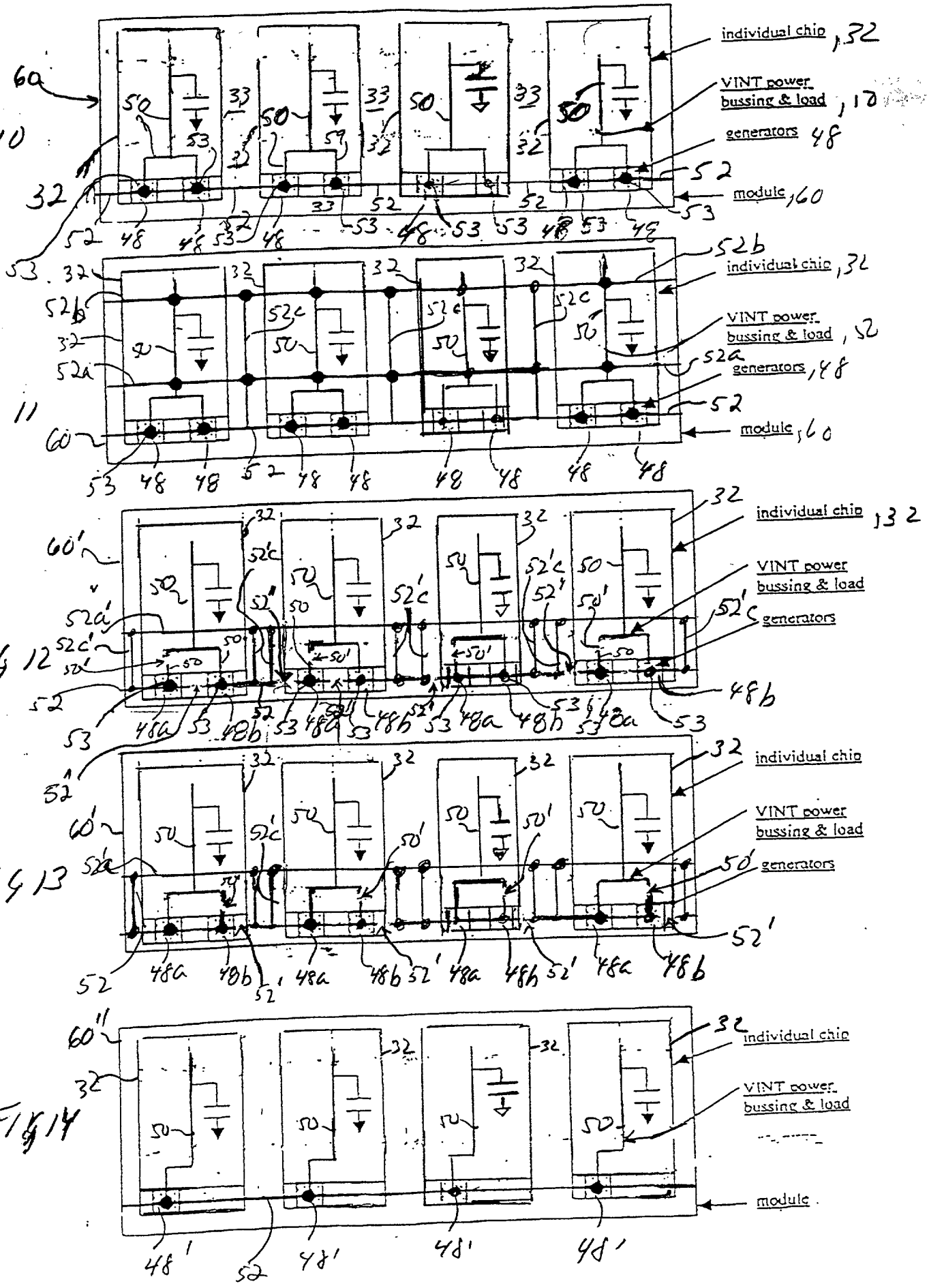


FIG. 10

FIG. 11

FIG 12

FIG 13

FIG 14

DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe we are the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR ARRANGEMENT

the specification of which
_x_ is attached hereto, and
___ was filed on _____ as Application Serial No. _____
and was amended on _____ (if applicable)

Listing of named inventor(s): Manfred REITHINGER, Mike KILLIAN, Gerd FRANKOWSKY, Oliver KIEHL, Gerhard MUELLER, Ernst STAHL, Hartmund TERLETZKI, and Thomas VOGELSANG

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Codes, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIOR FOREIGN APPLICATION(S)			Priority claimed	
(Number)	(Country)	(Day/month/year filed)	Yes	No
(Number)	(Country)	(Day/month/year filed)	Yes	No
(Number)	(Country)	(Day/month/year filed)	Yes	No

I hereby claim the benefits under Title 35, United States Code, § 120 and/or 119 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, we acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing date)	(Status) (patented,pending,abandoned)
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Power of Attorney: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Adel A. Ahmed, Reg. No. 29,606; I. Marc Asperas, Reg. No. 37,274; Stanton C. Braden, Reg. No. 32,556; Robert T. Canavan, Reg. No. 37,592; Dexter K. Chin, Reg. No. 38,842; Joseph S. Codispoti, Reg. No. 31,819; Lawrence C. Edelman, Reg. No. 29,299; Mark H. Jay, Reg. No. 27,507; Stuart Kaler. Reg. No. 35,913; Rosa S. Kim, Reg. No. 39,728; Peter A. Luccarelli, Jr., Reg. No. 29,750; Jeffrey P. Morris, Reg. No. 25,307; Pasquale Musacchio, Reg. No. 36,876; Donald B. Paschburg, Reg. No. 33,753; Laura Slenzak, Reg. No. 33,363; Darryl A. Smith, Reg. No. 37,756; Daniel J. Staudt, Reg. No. 34,733; Erik C. Swanson, Reg. No. 40,194;Heather S. Vance, Reg. No. 39,033; Scott T. Weingaertner, Reg. No. 37,756; Robert A. Whitman, Reg. No. 36,966; Ira Lee Zebrak, Reg. No. 31,147

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Direct telephone calls to:

Elsa Keller, Legal Administrator (732) 321-3026

I hereby declare that all statements made herein on my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Full name of sole or first inventor	Manfred REITHINGER
Inventor's signature	Manfred Reithinger Manfred Reithinger
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Citizenship	United States
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Inventor's signature	
Date	
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Full name of fourth inventor	Oliver KIEHL
Inventor's signature	Oliver Kiehl
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Date	
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Full name of eighth inventor	Thomas VOGELSANG
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Post Office Address	12 Murray Lane, Jericho, Vermont 05465

DECLARATION FOR PATENT APPLICATION & POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe we are the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

SEMICONDUCTOR ARRANGEMENT

the specification of which
_x_ is attached hereto, and
___ was filed on __________ as Application Serial No. _____________
and was amended on ___________ (if applicable)

Listing of named inventor(s): Manfred REITHINGER, Mike KILLIAN, Gerd FRANKOWSKY, Oliver KIEHL, Gerhard MUELLER, Ernst STAHL, Hartmund TERLETZKI, and Thomas VOGELSANG

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